



PATENT

IN THE UNITED STATES PATENT OFFICE

Applicants: Jason H. Anderson et al.
Assignee: Xilinx, Inc.
Title: Post-Layout Optimization in Integrated Circuit Design
Serial No.: 10/644,132 File Date: 08/20/2003
Examiner: Binh C. Tat, Art Unit: 2825
Docket No.: X-946 US Conf. No.: 5337

Mail Stop AMENDMENT
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The enclosed reference(s) is/are being cited after the receipt of a first office action but prior to any final action.

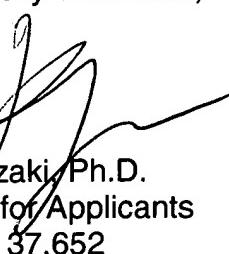
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Respectfully submitted,

12/23/2005 DTESEM1 00000016 240040 10644132

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I hereby certify that this correspondence is being deposited with the United States Postal Service as **first class mail** in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on December 19, 2005.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application / Conf. No.	10/644,132	/ 5337
(use as many sheets as necessary)		Filing Date	August 20, 2003	
		First Named Inventor	Jason H. Anderson	
		Art Unit	2825	
		Examiner Name	Binh C. Tat	
Sheet	1	of	1	Attorney Docket Number
				X-946 US

OTHER - NON PATENT LITERATURE DOCUMENTS

Examiner Signature		Date Considered	
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